Eur. Phys. J. B **23**, 421–425 (2001)

THE EUROPEAN PHYSICAL JOURNAL B

EDP Sciences
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Springer-Verlag 2001

Whole-wafer fabrication process for three-terminal double stacked tunnel junctions

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Received 5 June 2001

Abstract. A new fabrication process for three-terminal superconducting devices consisting of two Josephson junctions in a stacked configuration is reported. The process is based on the deposition of the whole $Nb/Al_xO_y/Nb$-$Al/Al_xO_y/Nb$ multilayer on a Si crystalline wafer without any vacuum breaking. Lift-off techniques, anodization processes and a SiO film deposition have been adopted for patterning and insulating the two tunnel stacked junctions. Devices have been characterized in terms of current-voltage (I-V) curves and Josephson critical current *vs.* the externally applied magnetic field. They show high quality factors (V_m values up to 65 mV at 4.2 K), and good current uniformity.

PACS. 74.50.+r Proximity effects, weak links, tunneling phenomena, and Josephson effects – 85.25.Am Superconducting device characterization, design, and modeling

1 Introduction

In the recent past some efforts have been devoted to the development of three-terminal superconducting devices based on stacked tunnel structures due to their transistor-like behavior at low temperatures. Among them, devices based on low-T_c superconductors seems to be very promising to provide high gains [1–4]. In particular the quasi-particle trapping transistor, based on quasi-particle trapping from a superconductor into a normal metal in a double tunnel junction configuration, proposed by Oxford and Naples groups [5,6], appears to be very attractive in the field of superconducting electronics.

In this context, since 70th years three-terminal devices based on non-equilibrium superconductivity have been proposed and realized. The transistor-like device presented in reference [1] consisted of two superimposed superconducting tunnel junctions, realized by using metallic masks by a shadow evaporation technique. The fabrication process required the vacuum breaking at different steps, and the use of varnish layers for isolation of electrodes. As a consequence, realized structures had large area (about 1 mm^2) and their quality was strongly influenced by impurities absorbed at the interfaces during the vacuum breaking. Nevertheless, this process was not particularly suitable for large scale integration and hybrid electronics.

In the 80th years many processes for the fabrication of high quality all-refractory single Josephson junctions were developed [7–9]. They were mostly based on a whole-wafer process consisting of a large trilayer structure deposited without vacuum breaking, and the subsequent definition of single junctions by optical lithography, dry and wet etchings. These techniques were also extended to fabricate three terminal double tunnel junction devices with a planar structure [10,11]. These configurations have been largely used for investigating non-equilibrium properties occurring in superconducting tunnel junctions such as the measurement of the quasi-particle diffusion constant [10–12]. However, toward the development of fast electronics characterized by short charge transfer times at low temperatures, a stacked configuration could be much more attractive. In fact, in this geometry the crossing time through the thin intermediate electrode can be very small, and hence the bandwidth very large. Many three-terminal stacked configurations have been realized by using several advanced processes based anyway on separated fabrication steps for each junction [13,14]. Nevertheless, the vacuum breaking, occurring between depositions for different junctions, can influence the superconducting properties of the realized devices due to impurities localized at the surface, the physical stress produced by sputter-cleaning processes, etc.

In this paper we propose a Whole-wafer Three-terminal Stacked Devices (WTSD) fabrication process

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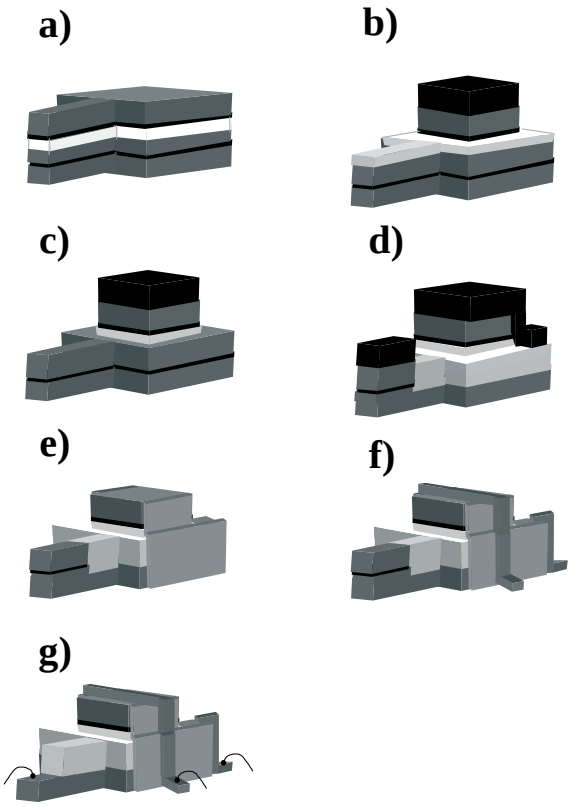

Fig. 1. Schematics of the various fabrication steps. a) Deposition of the multilayer; b) etching of the Nb and the top barrier by R.I.E.; c) etching of Al; d) chemical anodization of the Nb bottom; e) isolation by SiO; f) wiring process; g) definition of the bottom lead.

based on the deposition of the whole multilayer structure without any vacuum breaking. This new fabrication process allows to overcome the above discussed drawbacks of old fabrication processes leading to clean interfaces into the intermediate electrode. An extensive description of the fabrication process and preliminary results concerning the characterization of the realized devices are reported in the following sections.

2 Fabrication process

The multilayer $Nb/Al_xO_y/Nb\text{-}Al/Al_xO_y/Nb$ was deposited on a 2-inch Si crystalline wafer and patterned by using the lift-off technique as shown in Figure 1a. Both the niobium and aluminum films were deposited by using dc sputtering magnetron sources in a ultra-high vacuum system at a base pressure of 10^{-8} torr. In both cases the Ar dynamic pressure during the sputtering was kept to 3.5 mtorr, while the deposition rates were 1.5 nm/s and 0.09 nm/s for Nb and Al respectively. The temperature of the substrate was not controlled. The thicknesses of different layers are reported in Table 1. The Al_xO_y tunnel barriers were obtained by thermal oxidation of the Al film

Table 1. Fabrication parameters.

	Material	Thickness [nm]
Bottom electrode	Nb	150
	Al	10
Tunnel barrier	Al_xO_y	-
Intermediate electrode	Nb	40
	Al	10 (device 1)
		20 (device 2)
		30 (device 3)
Tunnel barrier	Al_xO_y	-
Top electrode	Nb	50
Wiring	Nb	350

surface in pure oxygen gas. The Josephson critical current density was controlled both by the oxygen gas pressure and the oxidation time. Typically a value of about 2.5×10^4 Pa oxygen gas pressure for 1 hour produces a Josephson current density of the order of 100 A/cm^2. For the lift-off process we used a μm thick resist layer soaked for few minutes in chlorobenzene between the exposure and its development to get the overhanging step profile. The resist was removed by conventional soaking in acetone. A lift-off technique, instead of a whole-wafer etching process, has been adopted in order to avoid the etching of large area of the multilayer for the definition of both electrodes and junction area.

The next step of the photolithographic process defines the area of the top junction (see Fig. 1b). The Nb top layer was dry etched by a Reactive Ion Etching process (R.I.E.) carried out at room temperature in a CF_4 gas atmosphere at 450 mtorr and an O_2 gas atmosphere at 20 mtorr at 50 W with an etching rate of 50 nm/min. Afterward, without removing the photoresist, the Al_xO_y and the Al films into the intermediate electrode were chemically etched (Fig. 1c). The area of the bottom junction was defined by using the anodization oxide growth down to the Nb of the base electrode (Fig. 1d). The anodization process was done at room temperature in an electrolyte solution of ammonium pentaborate and ethylene glycol. It was carried out at a constant current with a rate of 0.5 nm A/s The mask for the anodization process was designed in such a way that only a small depth of the peripherical Nb was transformed into Nb_xO_y oxide leaving the junction area almost unchanged. Before the wiring deposition for both intermediate and top electrode, an insulation layer of SiO was deposited on the periphery of the top tunnel barrier and patterned by lift-off technique (Fig. 1e). The insulation layer of SiO was thermally deposited in a separate UHV system at a base pressure of 5×10^{-7} torr by using a chimney-type furnace boat at a rate of 2 nm/s. Finally, after a sputter-etching cleaning of the film surfaces, the Nb wiring for the electrical contact of both intermediate and top electrode was deposited and patterned by lift-off technique too (Fig. 1f). The Nb wiring

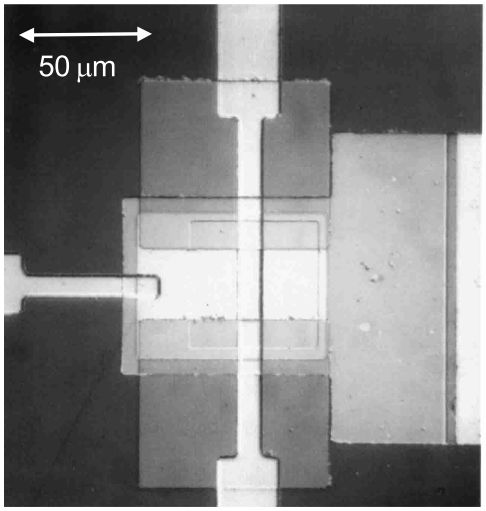

Fig. 2. Photo of a single three-terminal device. The area of the top and bottom junction are 50×50 μm^2 and 50×75 μm^2 respectively, the size of the base electrode is 120×400 μm^2.

was deposited at the rate of 2.5 nm/s. In order to avoid any problem during the removal of the photoresist in the following lift-off process, a Nb film (50 nm) was deposited in two steps, each of 25 nm, separated by 30 minutes of cooling. Finally, the geometry of the bottom lead was defined both by R.I.E. of the intermediate Nb layer and wet etching of the bottom tunnel junction (Fig. 1g).

Each wafer includes nine 5×5 mm^2 chips, each containing several three-terminal devices in different configurations with junction area ranging from 5×5 μm^2 to 100×100 μm^2 and electrodes with different size. A photograph of a three-terminal device fabricated by the above process is shown in Figure 2. In this device the bottom junction has an island-type geometry, whereas the top is a window-type junction. The top electrode is common to all realized devices. The width of the wiring contact ranges from 3 μm to 10 μm depending on the junction area, while the size of the bottom electrode not covered by the tunnel barrier ranges from 50×400 μm^2 to 120×400 μm^2. Devices with different thicknesses of the intermediate bilayer have been realized. In particular, we will present experimental results for stacked devices with different configurations of the intermediate electrode, which consisted of Nb (50 nm) and Al, whose thickness ranged from 10 nm to 30 nm. These structures are currently used for experiments concerning both the proximity and quasi-particles trapping effects in bilayers of thin films.

3 Results and discussion

The reported fabrication process takes advantages of a fine control of the deposition procedures for Nb and Al films and of a high degree of barrier uniformity. The process is well settled for the fabrication of single Josephson junctions and SQUIDs [15]. The three-terminal superconducting stacked devices have been characterized by measuring the current-voltage (I-V) curves at different temperatures down to 1.5 K for bottom, top and in series connected double junctions. All measurements were performed in a shielded environment by using cryoperm cans just around the sample. The temperature was changed through a fine control of the vapor pressure. The I-V curves were recorded by using a computer controlled data acquisition system.

We tested several junctions with different area and different relative thickness of the intermediate bilayer. Typical I-V curves at $T = 4.2$ K are reported in Figure 3. The I-V characteristics of bottom junctions are almost independent on the relative thickness of Nb/Al films in the intermediate electrode. They show a high quality factor $V_{\rm m} = 0.7\ \Delta I_{\rm g} R_{2{\rm mV}}$ (where $\Delta I_{\rm g}$ is the current jump at the sum gap voltage and $R_{2{\rm mV}}$ the static resistance a $V = 2$ mV) up to 65 mV and a sum gap value of 2.80 mV. Moreover, different chips realized on the same wafer and in different photolithographic processes exhibited a reasonable reproducibility. The Josephson current density was about 80 A/cm^2.

On the other hand the electronic properties of the top junctions are strongly influenced by the presence of the proximity effect in the intermediate electrode. The sum gap voltage ranges from $V_{\rm g} = 2.5$ mV, in the case of an intermediate bilayer Nb(40 nm)/Al(10 nm), to $V_{\rm g} = 2.30$ mV at larger Al thickness. A difference of the gap voltages between two electrodes in the top junction was also observed at 700 μV (see Fig. 3d). The proximity effect is also responsible for higher sub-gap currents in the I-V curves, even if higher contribute from leakage currents produced by a not complete isolation of the SiO film can not be disregarded.

The devices have been characterized also in terms of magnetic field dependence of the Josephson current. The magnetic field was supplied by a Cu coil producing a magnetic field parallel to the tunnel barrier. Both bottom and top junctions show a Fraunhofer-like behavior for junction area lower than 50×50 μm^2. A typical $I_{\rm c}$-H curve at $T = 1.2$ K for a 50×50 μm^2 bottom junction is reported in Figure 4. The occurrence of well defined zero values for the minima of the pattern ensures a high uniformity of the barrier and the absence of effective structural fluctuations. A value of 45 μm for the Josephson penetration depth $\lambda_{\rm J}$ has been estimated. Larger area Josephson junctions show slightly asymmetric magnetic patterns due also to the presence of a superconducting ground plane effect and a not completely in-line geometry of current distribution [16].

Due to their physical characteristics, the realized devices are particularly suitable for investigating underlying physics concerning the role of the proximity effect in thin superconducting bilayers. In fact, the possibility to measure the I-V curves of top and bottom junction allows to infer about the effective density of states at both side of the bilayer's interface. This is very important toward the effective evaluation of non-equilibrium relaxation rates

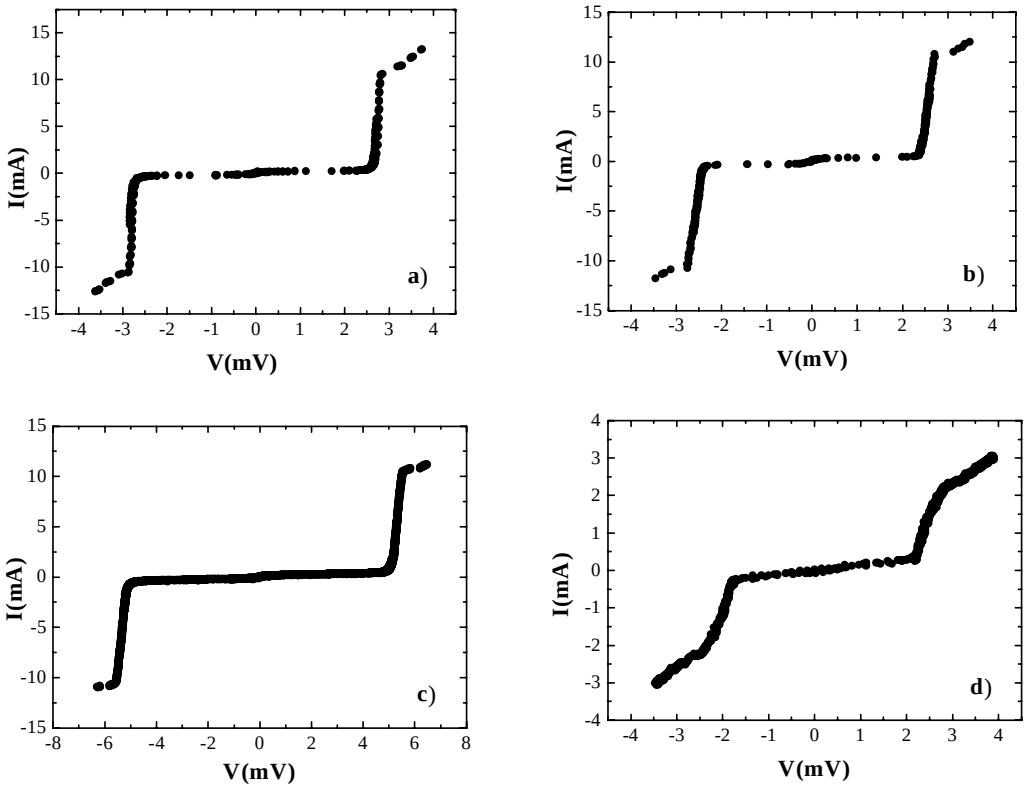

Fig. 3. I-V curves of bottom (a), top (b) and stacked (c) junction for Al = 20 nm and top junction for Al = 30 nm (d).

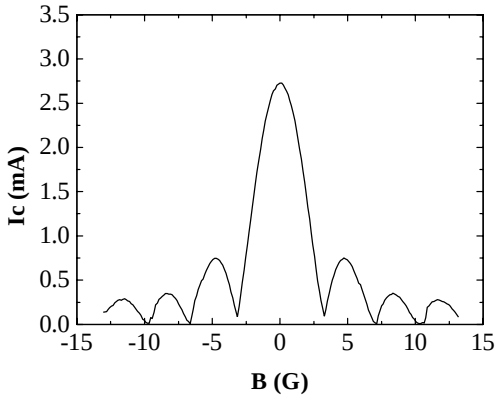

Fig. 4. I_c *vs.* B for a 50×50 μm^2 bottom junction at $T = 1.2$ K.

in proximised structures under the influence of an electronic perturbation. Moreover, the possibility to control the non-equilibrium regime through the quasi-particle injection from one of the two junctions can be very useful to study physical properties of proximised devices, based on the trapping effect, employed in many nuclear cryogenic applications [17]. The realized devices can be very interesting also in the development of both superconducting analogue and digital electronics. Besides the large scale integration they seems to be very promising in the realization of three-terminal devices operating as transistor-like amplifiers [6] or basic logical devices [18].

4 Conclusion

Three-terminal superconducting devices consisting of two Josephson junctions in a stacked configuration have been fabricated based on the whole $Nb/Al_xO_y/Nb$-$Al/Al_xO_y/Nb$ multilayer deposition on a silicon crystalline wafer without any vacuum breaking. This new fabrication process, named Whole-wafer Three-terminal Stacked Devices (WTSD), allows to overcome the difficulties related to the presence of impurities at the interfaces between films constituting the intermediate and bottom electrodes and also to avoid stress of these films induced by sputter-cleaning process. High quality three-terminal devices have been obtained where single junctions showed V_m values up to 65 mV at $T = 4.2$ K. The realized devices are particularly suitable for investigating the role of both proximity and trapping effect in bilayers under the influence of a injection-based perturbation. The presented process can led to benefits in the realization of three-terminal superconducting structures potentially compatible with hybrid large scale integrated electronics.

The authors would like to thank Prof. A. Barone and N.E. Booth for useful discussions. Technical assistance in the design

of photolitographic masks of Dr. G. Ammendola is also acknowledged. This work is partially supported by the I-MURST COFIN99 program "Low Temperature Detectors for high Resolution X-ray Spectroscopy".

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